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AGILENT TECHNOLOGIES
Legal Department, 51U-PD
Intellectual Property Administration
P.O. Box 58043
Santa Clara, CA 95052-8043

EXAMINER	
AGGARWAL, YOGESH K	

ART UNIT	PAPER NUMBER
2615	

DATE MAILED: 09/27/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/834,061	POST, WILLIAM L.	
	Examiner	Art Unit	
	Yogesh K Aggarwal	2615	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1-9,11-18 and 20* is/are rejected.

7)☒ Claim(s) *10 and 19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 April 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *04/7/2001, 4/11/01*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Specification

1. The disclosure is objected to because of the following informalities:

Paragraph 40, index manager 242 is not disclosed in the drawings.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-8, 11, 12 and 16-18 are rejected under 35 U.S.C. 102(b) as being anticipated by Katoh et al. (US Patent # 5,796,430).

[Claim 1]

Katoh et al. teaches a method for correcting at least one defective pixel (col. 3 lines 59-63) comprising: a) receiving a current pixel location (col. 5 lines 14-15, figure 2, S208); b) receiving a defective pixel location (col. 5 lines 24-26); c) determining whether the current pixel location is a defective pixel location (col. 4 lines 25-36); d) when the current pixel location is not a defective pixel location, providing a received pixel value as output pixel value (col. 5 lines 50-51, figures 6-8); and e) when the current pixel location is a defective pixel location, providing a previous pixel value as the output pixel value (col. 5 lines 42-50, figure s 6-8).

[Claim 2]

Katoh teaches that the current pixel location includes a current row and a current column, wherein the defective pixel location includes a defective pixel row and a defective pixel column

(col. 4 lines 36-53, col. 5 lines 21-29, figures 5 and 6) wherein the step of determining whether the current pixel location is a defective pixel location further comprises: 1) comparing the current row with the defective pixel row and comparing the current column with the defective pixel column (col. 5 lines 14-15, figure 2); 2) determining whether there is a match between the current row and column the defective pixel row and column (col. 5 lines 16-18, figure 2, the output of step 208).

[Claim 3]

Katoh teaches the step of when the current pixel location is not a defective pixel location, providing a received pixel value as an output pixel value further comprises receiving a pixel value from an analog to digital converter and providing the received pixel value as an output pixel value (figure 1 shows the noise correction circuit 107 receiving a pixel value from an A/D converter 106 and figure 8d disclose an output signal A_{11} when it is determined that the pixel is not a defective pixel).

[Claim 4]

Katoh teaches the step of when the current pixel location is a defective pixel location, providing a previous pixel value as the output pixel value further comprises 1) providing a previous pixel value that is in the same frame, in the same row, and a predetermined number of pixels from the current pixel location as the output pixel value (See figures 6-8).

[Claim 5]

Katoh teaches the step of providing a previous pixel value that is in the same frame, in the same row, and a predetermined number of pixels from the current pixel location as the output pixel value further comprises providing a previous pixel value that has the same color as the current

pixel (col. 5 lines 52-56). Katoh also teaches replacing a defective pixel value with a signal of the same color filter (col. 5 lines 53-55). The Examiner notes that if a Bayer pattern color filter is used then replacing the defective pixel with the same color filter means replacing it with a pixel value that is two locations to the left of the current defective pixel.

[Claim 6]

Katoh does not specifically teach the step of when the current pixel location is one of the first pixel location and the second pixel location of a row, providing a zero pixel value as the output pixel value. However such an arrangement would be a design choice to replace a first pixel or a second pixel with a zero if that is found to be defective because there is no previous pixel available for replacement. The first or the second pixel can be replaced with a zero or one depending upon the designer specifications.

[Claim 7]

Katoh teaches when the current pixel location is a defective pixel location, providing a previous pixel value as the output pixel value further comprises 1) employing a two step delay circuit (figure 10, element 1001 and 1002) to provide a replacement value for the defective current pixel. It would be inherent that the two-step delay circuit is reset to zero at the beginning of every row in order to refresh the circuit with a fat zero (or reset).

[Claim 8]

Katoh teaches the step of determining whether the current pixel location is a defective pixel location further comprises employing a memory for storing a plurality of defective pixel locations (col. 4 lines 36-53) and accessing the memory for defective pixel locations (col. 5 lines 24-29) wherein the defective pixel locations are predetermined and wherein the memory

provides a detection of defective pixels that is consistent from frame to frame and wherein artifacts that stem from an inconsistent defective pixel detection are eliminated (The threshold level against which the pixels are compared to determine whether it is a defective pixel is dependent upon temperature (col. 2 lines 14-21) and is therefore consistent from frame to frame assuming temperature is constant for a set of frames. Although Katoh teaches a memory and not a look-up-table, dual mode usage of Look-up-table SRAM cell to provide either a logic function or memory function has been very well known in the art for FPGA devices).

[Claim 11]

This is an apparatus claim corresponding to method claims 1,4,8 respectively. Therefore claim 11 is rejected based upon method claims 1,4,8 respectively.

[Claim 12]

This is an apparatus claim corresponding to method claim 2. Therefore claim 11 is rejected based upon method claim 2.

[Claims 16 and 18]

These are apparatus claims corresponding to method claims 3 and 4 respectively. Therefore claims 16 and 18 are rejected based upon method claims 3 and 4.

[Claim 17]

This is an apparatus claim corresponding to method claim 5. Therefore claim 17 is rejected based upon method claim 5.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Katoh et al. (US Patent # 5,796,430) in view of Balz et al. (US Patent # 5,929,865).

[Claim 9]

Katoh teaches the step of employing a table for storing a plurality of defective pixel locations includes storing the defective pixel locations (figure 1, element 110) but fails to teach storing the defective pixels in a sorted order wherein a search of the table to determine if a current pixel location is a defective pixel location is obviated. However Balz et al. teaches storing pixels in a sorted order (col. 4 lines 20-23) in order to obviate the search for locating a defective pixel. The Examiner notes that these pixels may be defective pixels. Therefore taking the combined teachings of Katoh and Balz, it would have been obvious to one skilled in the art at the time of the invention to store the defective pixels in a sorted order. The benefit of doing so would be so that the search is less time consuming than the conventional methods.

6. Claims 13-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Katoh et al. (US Patent # 5,796,430) in view of Dong (US Patent # 6,665,009).

[Claim 13]

Katoh fails to teach, "an index manager coupled to the table and the match unit for receiving the match signal and responsive thereto for managing a table index that points to a current defective pixel location in the table". However Dong discloses a signal processor 110 (figure 3) that is coupled to the location storage 130 (figure 3) and the location comparator (140) wherein the

dead pixel comparator points to a current defective pixel location in the location storage (col. 4 lines 1-8). Therefore taking the combined teachings of Katoh and Dong, it would have been obvious to one skilled in the art at the time of the invention to have an index manager (signal processor 110) coupled to the table (location storage) and the match unit (140) for receiving the match signal and responsive thereto for managing a table index that points to a current defective pixel location in the table in order to locate the defective pixel. The benefit of doing so would be to locate a current defective pixel location in the table with a small location storage circuitry.

[Claim 14]

Dong teaches wherein the index manager (figure 3, element 110), responsive to an asserted match signal (col. 4 lines 9-22), increments the table index so that the table index points to the next defective pixel location (col. 5 lines 3-7); and wherein the index manager has an input for receiving a start frame signal and responsive thereto for resetting the table index (figure 4b, box 250)

[Claim 15]

Katoh fails to teach, "wherein the defective pixel detection mechanism includes a register coupled to the table for use in writing defective pixel locations to the table and reading defective pixel locations from the table". However Dong discloses a location shift register (figure 3, element 150) used to write defective pixel locations to the table and reading defective pixel locations from the table (col. 3 lines 57-67). Therefore taking the combined teachings of Katoh and Dong, it would have been obvious to one skilled in the art at the time of the invention to have a defective pixel detection mechanism that includes a register coupled to the table for use in writing defective pixel locations to the table and reading defective pixel locations from the table

in order to write and read the defective pixel location into the memory. The benefit of doing so would be that a single shift register, which consumes relatively less area on the chip, could be used to do both write and read functions.

7. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Katoh et al. (US Patent # 5,796,430).

[Claim 20]

Katoh teaches (a) a sensor array having a plurality of pixels arranged in rows and columns (figure 1, element 104); wherein at least one pixel is defective (figure 4); (d) a timing controller coupled to the sensor array for providing control signals thereto (figure 1, element 103); (e) a defective pixel detection mechanism (figure 1, element 107) that employs a look-up table (figure 1, element 110) with defective pixel locations for providing a determination of whether a pixel is defective or non-defective that does not vary from frame to frame (col. 5 lines 42-51, figure s 6-8); and (f) a defective pixel correction mechanism (figure 1, element 107) coupled to the defective pixel detection mechanism that employs a consistent replacement choice facility for providing a previous pixel value in the same frame, on the same row, and a predetermined number of pixels from the current pixel location as a replacement value, and a replacement unit for replacing the defective pixel value with the replacement value (see figures 6-8). Katoh is silent regarding a (b) a row selector coupled to the sensor array for selecting a row of the sensor array; (c) a column selector coupled to the sensor array for selecting a column of the sensor array. However Official notice is taken of the fact that it is notoriously common to have a row and column selector coupled to the sensor array in order to select a row and column respectively of the sensor array. Therefore taking the combined teachings of Katoh and Official notice, it

would have been obvious to one skilled in the art at the time of the invention to have a row selector coupled to the sensor array for selecting a row of the sensor array and a column selector coupled to the sensor array for selecting a column of the sensor array in order to select any row or column depending upon the commands from the processor.

Allowable Subject Matter

8. Claims 10 and 19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

9. The following is a statement of reasons for the indication of allowable subject matter: The prior art fails to fairly suggest Katoh fails to teach " wherein the step of employing a table for storing a plurality of defective pixel locations includes setting the row value of the last entry in the table to a value that is greater than the first predetermined number of rows; and setting the column value of the last entry in the table to a value that is greater than the second predetermined number of columns; wherein hardware to determine if the last entry in the table has been reached is obviated".

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yogesh K Aggarwal whose telephone number is (703) 305-0346. The examiner can normally be reached on M-F 9:00AM-5:30PM.

10. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Andrew Christensen can be reached on (703) 308-9644. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

11. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

YKA
September 14, 2004

TUAN HO
PRIMARY EXAMINER